METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND SEMICONDUCTOR COMPONENT THEREOF

Field of the Invention

The present invention pertains to methods of making semiconductor components and the components thereof, and more particularly to bipolar transistors.

Background of the Invention

It is well known that bipolar transistors, especially heterojunction bipolar transistors (HBTs) based on GaAs technologies, can exhibit excessive current leakage at emitter/base contact junctions. See Lin, Hao-Hsiung et. Al., "Super-gain AlGaAs/GaAs Heterojunction Bipolar Transistors using an Emitter Edge-thinning design," Appl. Phys. Lett. 47 (8), 15 October l985, pp. 839-841. Surface recombination of electrons in the base material and the spacing between the emitter and base contacts of the devices degrade transistor performance and affect device reliability.

The prior art has attempted to minimize the parasitic capacitance at these emitter/base junction areas by, for example, producing devices 10 on a substrate 26. An area between the emitter layer 34 and the base contacts 48 is covered with a photoresist material 50 prior to etching the device as described in U. S. 5,804,877 (Fuller et. al.) and illustrated in Figure 1. The disadvantage of this method is the use of an additional photolithography step during the device fabrication process that

causes damage to collector sidewalls during the stripping of the photoresist and limits the useful operating voltage of the transistor.

To address the surface recombination problem that reduces the reliability of the HBTs, a fabrication process described in U. S. 5,001,534 (Lunardi et. al.) required that an emitter layer (referred to as a ledge) be left intact beneath the entire base contact and electrical contact to the base layer of the device was accomplished through the intact emitter layer. The base contact metal was diffused through the emitter layer, and the reliability of the transistors were compromised.

In U. S. 5,840,612 (Oki et. al.) surface passivation of HBTs was again addressed by using a depleted layer of widebandgap semiconductor (also referred to as a ledge) over the extrinsic base region of the transistor. The ledge thickness was defined by selectively etching away semiconductor layers above the widebandgap semiconductor; however, it is difficult to achieve a consistent ledge thickness and thus large variations in the device's characteristics result.

As demand for more reliable device performance continues to increase, the need for semiconductors, especially HBTs based on GaAs technologies, which exhibit maximum operating voltages has become apparent.

Accordingly, a need exists for a method of manufacturing a semiconductor component, and a semiconductor component thereof, that is both reliable and exhibits maximum operating voltages.

Brief Description of the Drawings

The present invention will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying drawing figures in which:

~~FIG. 1 is a cross-sectional view of a semiconductor component manufactured~~ according to the prior art method described above;

FIGs. 2 – 7 illustrate cross-sectional views of a semiconductor component during different stops of a manufacturing process in accordance with an embodiment of the invention;

FIG. 8 is a flowchart of the preferred process according to the invention.

For simplicity and clarity of illustration, the figures illustrate the general invention, and descriptions and details of well-known features and techniques are omitted to avoid excessive complexity. The figures are not necessarily drawn to scale, and the same reference numerals in different figures denote the same elements. It is further understood that the embodiments of the invention described herein are capable of being manufactured or operated in other orientations than described or illustrated herein.

Detailed Description of Preferred Embodiments

The present invention pertains to the fabrication of a semiconductor device, and in particular a heterojunction bipolar transistor, that eliminates the need for an additional photolithography step and thus avoids damage to the sidewalls of the collectors of the devices caused by photoresist stripping. The resulting devices reliably operate at voltages of up to about 30 volts.

In a preferred embodiment of the invention, an emitter-up configuration is described, though one may appreciate that a collector-up transistor may be similarly fabricated. The material structure is illustrated in FIG. 2. The transistor is fabricated using an epitaxial layer structure on a substrate or wafer 220, such as for example silicon, or InP or GaAs (both semi-insulating substrates). The substrate 220 includes a subcollector layer 240, preferably a GaAs layer that is approximately 0.5 μm thickness and doped with Si, for example, to a concentration of approximately 3 x 10^{18} cm $^{-3}$; a collector layer 260, preferably GaAs having a thickness of approximately 0.5 μm and doped with Si, for example, to a concentration of approximately 2.0 x 10^{16} cm^{-3} ; a base layer 270, preferably GaAs of approximately 0.08 μm in thickness and doped with carbon to a concentration of preferably approximately 4 x 10^{19} cm^{-3} ; an emitter layer 280, preferably of either AlGaAs or of GaInP, approximately 0.1 μm in thickness and doped with Si for example to a concentration of approximately 3 x 10^{17} cm^{-3} ; a buffer layer 290, preferably GaAs, approximately 0.15 μm in thickness and doped with Si, for example, to a concentration of approximately 3 x $10^{18}cm^{-3}$; a transition layer 295 of

approximately 0.05 μm in thickness and doped with Si, for example, to a concentration of approximately 3 x 10^{18} cm^{-3}, with composition varying smoothly from GaAs to InGaAs, preferably In0.5Ga0.5As; and an InGaAs cap layer 295 approximately 0.05 μm in thickness and doped with Si, for example, to a concentration of approximately 1 x 10^{19} cm^{-3}. A TiWN layer 310 is sputter-deposited on the InGaAs layer 295, as shown in FIG. 3.

The emitter geometry is formed by lift-off techniques in which the emitter pattern is formed as openings in a photoresist film. Photoresist 320 is spun to a thickness of approximately 1.2 μm followed by a track bake at about 100° C. for approximately 60 seconds. The wafer is then exposed in a stepper apparatus, and batch developed in a solution of 1:1, photoresist developer and water, for about 2 minutes. The exact conditions will vary with resist batch, as will the bakes, pattern exposure, and develop times for optimum resist sidewall profile also change. This process leaves a TiWN surface exposed in the desired location of the emitter contact, as shown in FIG. 3.

Following sequential evaporation of 0.05 μm Ti, 0.03 μm Pt, and 0.15 μm Au, the photoresist is lifted off in solvent, leaving the structure shown in FIG. 4. Typically, acetone is employed with soaks, ultrasonic agitation or spraying while the wafer is being spun. While the details of the lift-off process can adversely affect the patterning results, almost any process that leaves a debris-free surface is suitable. The resulting patterned metal 410 is used as a mask to etch the emitter geometry into the TiWN and then into the semiconductor underneath.

In order to form the emitter mesa of the transistor, a selective reactive ion etching (RIE) process is employed to etch through the TiWN 310, stopping on the InGaAs 295 surface; for example, CF4 + 8% O2 £ 250 watts, 30 millitorr, 40o C.,to a visible clearing of the TiWN layer 310 plus 50% over-etch. The InGaAs 295 is etched in a non selective, timed, wet etch (such as a 1:8:160 solution of H2SO4:H2O2:H2O for about 25 seconds) which results in the structure of FIG. 5. ~~The GaAs buffer 290 is etched in a process that stops on the emitter layer 280.~~ For an AlGaAs emitter, this can be achieved, for example, by RIE conditions of 80o C., 200 watts, 95 mT in gas flows of: 4.5% H2 in He, 20 sccm; CCl4, 10 sccm; alternatively, BCl3 + SF6 can be used instead. For a GaInP emitter, such selective etching can be achieved, for example, using the aforementioned 1:8:160 solution of H2SO4:H2O2:H2O, which does not etch GaInP.

One or more dielectric layers are then deposited. In a first preferred embodiment, the dielectric layer 620 consists of silicon nitride, silicon dioxide or silicon oxynitride, most preferably silicon nitride. Photoresist is applied and patterned to define a region of the emitter layer 280 as a ledge region 640. The ledge region 640 surrounds the emitter mesa in order to reduce surface recombination of electrons. The dielectric layer is removed outside the ledge region 640 by a reactive ion etch process. The photoresist is then removed by acetone spray and ash. Subsequently the emitter layer 280 is removed outside the ledge region 640, for example, by wet chemical etching, to expose the base layer 270, preferably p+, while forming an undercut region (AA) with a lateral extent of approximately 0.1 um by removal of a

portion of the emitter layer 280 under the dielectric layer. For an emitter layer 280 composed of AlGaAs, the aforementioned 1:8:160 solution of H2SO4:H2O2:H2O may be used for this etch; for a layer composed of GaInP, a 3:1 solution of H3PO4 : HCl may be used. A photoresist pattern is made with a process similar to that described for the lift off patterned emitter contact geometry. This photoresist pattern overlaps the ledge region 640, so that the pattern exposes an area of the base layer 270 and an immediately adjacent area of the dielectric covering the ledge region 640. Ti-Pt-Au films , in thicknesses of 500, 300, and 1500 Angstroms are sequentially evaporated and lifted off to form a base contact 660. This base contact 660 lies directly on the base layer 270 adjacent to the ledge region 640, and also overlaps onto the dielectric layer 620 covering the ledge region 640. The undercut region (AA) separates the base contact 660 from the emitter layer 280 to prevent an undesirable electrical connection between the base contact 660 and the emitter layer 280. The structure, with the base contacts 660, is shown in FIG. 6.

A base mesa is etched through the base layer 270 and the collector layer 260 to expose the subcollector layer 240, preferably n+, using the overlapping base contact 660 and dielectric layer 620 in the ledge region 640 as an etch mask to minimize base collector capacitance. The base mesa etch process may use, for example, a 1:8:160 solution of H2SO4:H2O2:H2O with an etch time appropriate for the base layer 270 thickness plus the collector layer 260 thickness

In a second preferred embodiment which utilizes a reactive ion etch process to form the base mesa instead of a wet chemical etch as was used in the first preferred

embodiment, the dielectric layer 620 consists of sequentially-deposited silicon nitride; aluminum nitride; and silicon nitride, silicon dioxide or silicon oxynitride. This dielectric stack allows patterning of aluminum nitride while not requiring aluminum nitride to be in direct contact with semiconductor surfaces or photoresist, as such contact could cause undesirable interactions. Photoresist is applied and patterned to define a ledge region 640 surrounding the emitter mesa. The upper silicon nitride layer is removed by a reactive ion etch process to expose the aluminum nitride layer outside the ledge region 640. The photoresist is then removed by acetone spray and ash, and the exposed aluminum nitride is etched using the patterned silicon nitride layer as a mask. Aluminum nitride can be etched using alkaline solutions such as a 10 : 1 solution of H_2O : NH_4OH. The remaining exposed silicon nitride, both inside and outside the ledge region, is then removed by reactive ion etch. Although the described embodiments utilize silicon nitride and aluminum nitride, other dielectric materials, including but not limited to silicon dioxide, silicon oxynitride, and polyimide, may be employed instead of or in combination with silicon nitride and aluminum nitride. Processes similar to those described in the first preferred embodiment may be employed to remove the emitter layer 280 outside the ledge region 640, form undercut region (AA), and form a base contact 660 which overlaps onto the dielectric layer 620 covering the ledge region 640. A base mesa is etched through the base layer 270 and the collector layer 260 to expose the subcollector layer 240, preferably n+, using the overlapping base contact 660 and the dielectric layer 620 in the ledge region 640 as an etch mask to minimize base collector capacitance. The base mesa etch process may use, for

example, a reactive ion etch with BCl3 + SF6, which etches GaAs with high selectivity with respect to aluminum nitride.

Collector contact 720 is formed using a photoresist liftoff process similar to that described for forming the emitter layer 280 and the base contacts 660. AuGe/Ni/Au contact metallization is evaporated over the photoresist-patterned wafer, and solvent lift-off is employed to remove the resist and the excess metal. Wafers are then ashed to remove the final organic residues. The resulting structure is shown in FIG. 7.

Electrical contacts and interconnections are made to emitter, base and collector regions. Interconnects are brought into these regions through vias in partially planarized dielectrics.

Therefore, an improved method of manufacturing a semiconductor component and the resulting component are provided to overcome the disadvantages of the prior art. The semiconductor components have more reliable performance and exhibit maximum operating voltages.

Although the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes may be made without departing from the spirit or scope of the invention. For instance, the numerous details set forth herein such as, for example, material compositions, chemical concentrations, and layer thicknesses are provided to facilitate the

understanding of the invention and are not provided to limit the scope of the invention. Accordingly, the disclosure of embodiments of the invention is intended to be illustrative of the scope of the invention and is not intended to be limiting. It is intended that the scope of the invention shall be limited only to the extent required by the appended claims.